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10/629,167

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use several sheets if necessary)

Applicant: Huy Nguyen, et al.

Filing Date:
07/28/03

Group:
2819



U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
DC	5,534,795	07/09/96	Wert et al.	326	81	12/09/94
DC	5,534,798	07/09/96	Phillips et al.	326	108	06/06/95
DC	5,663,663	09/02/97	Cao et al.	326	81	04/26/96
DC	5,751,168	05/12/98	Speed, III et al.	326	83	04/28/95
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DC	5,867,010	02/02/99	Hinedi et al.	323	282	06/06/97
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DC	6,160,421	12/12/00	Barna	326	63	10/22/98

EXAMINER

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FOREIGN PATENT DOCUMENTS

		Document Number							Date	Country	Class	Subclass	Translation	
													Yes	N

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

DL			"Direct Rambus Clock Generator", Rambus Inc., Document DL-0056, Version 1.2, November 2000, pages 1-22.
DL			"Application Brief #1", IDT Logic Applications, Integrated Device Technology, Inc., APP-BRF1-00050, 2000, pages 1-4.
DL			Jim Hagerman, "Two Transistors Form Bidirectional Level Translator", www.ednmag.com/reg/1996/110796/23DI_02.htm , 1996, pages 1-3.
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DL			"System Management Bus (SMBus) Specification Version 2.0", Section 2 General Characteristics, SBS Implementers Forum, August 3, 2000, pages 9-10.
DL			Kenneth M. Cuy, "Design Considerations Bring Unity To A Mixed-Voltage World", www.ednmag.com/ednmag/reg/1995/020295/03df3.htm , February 2, 1995, pages 1-8.
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